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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/208,105	11/25/1998	KAZUHISA SAKAMOTO	10233.81USW1	7685

7590 01/11/2006

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/11/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/208,105
Filing Date: November 25, 1998
Appellant(s): SAKAMOTO, KAZUHISA

Curtis Hamre
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 26, 2005 appealing from the Office action mailed 12/16/2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,808,352	Sakamoto	9-1998
5,981,981	Takahashi	11-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto.

Sakamoto teaches in figure 1 and related text a semiconductor device comprising:

a substrate 10, 11 having regions (region 21 and regions on the left and right to region 21) irradiated with radiating rays,

crystal defects 21 within the regions irradiated,

impurity regions 12, 13 in the substrate, and

a light metal wiring layer 18, 19 comprising aluminum located over the substrate except at openings above the regions irradiated and being connected to each of the impurity regions, wherein radiating rays passing to the regions irradiated through the openings generate the crystal defects under the openings so that a smaller amount of

radiating rays are irradiated elsewhere in the substrate as compared with said regions under the openings.

Sakamoto does not state that the metal wiring layer is located over the entire substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the metal wiring layer over the entire substrate, in Sakamoto's device in order to simplify the processing steps of making the device. The processing steps of making the device would be simplified by depositing the metal wiring layer over the entire substrate and etching the required openings, instead of complicating the processing steps by providing special masks in order to form the metal wiring layer only over selected sections of the substrate.

Regarding claim 10, Sakamoto teaches a metal wiring layer formed in a thickness so the smaller amount of radiating rays are irradiated elsewhere in said substrate, except the regions under the openings.

Regarding claims 11 and 12, Sakamoto teaches in figures 1 an insulation layer being formed above the regions irradiated, the openings being on the insulating layer, and the metal wiring 18, 19 covers part of the insulating layer.

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Takahashi.

Sakamoto teaches substantially the entire claimed structure, as applied to claims 9-12 above, except using the invention in an IGBT and a MOSFET semiconductor device, wherein the impurity region is a source region. Takahashi teaches in figure 30 an IGBT and a MOSFET semiconductor device, wherein the impurity region is a source region. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Sakamoto's invention in an IGBT and a MOSFET semiconductor device, wherein the impurity region is a source region in order to use the invention in an application which requires an IGBT and a MOSFET semiconductor device. The claimed limitation of a radiated region being a positive-negative junction where a parasitic diode is generated is inherent in prior art's device.

(10) Response to Argument

1. Appellant argues that Sakamoto uses silicon nitride 17 over the entire substrate and not the metal wiring electrodes 17, 18, as recited in claim 9.

Sakamoto uses silicon nitride 17 to control the amount of crystal defects in the semiconductor layer 11. However, claim 9 recites:

"a metal wiring layer located over the entire substrate except at openings above the regions irradiated, wherein

radiating rays passing to the regions irradiated through the openings generate the crystal defects under the openings, and

so that a smaller amount of radiating rays are irradiated elsewhere in the substrate as compared with said regions under the openings."

Figure 1 of Sakamoto clearly depicts the metal wiring layer 18, 19 located over the substrate except at openings above the regions irradiated, wherein

radiating rays must pass to the regions irradiated through the openings in order to generate certain amounts of crystal defects under the openings.

Regarding the claimed limitations of "a smaller amount of radiating rays are irradiated elsewhere in the substrate as compared with said regions under the openings", these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In any event, even if smaller amount of radiating rays are irradiated elsewhere in the substrate as compared with said regions under the openings in Sakamoto's device, the effect on Sakamoto's structure would be lack of crystal defects elsewhere in the substrate as compared with said regions under the openings. Lack of crystal defects elsewhere in the substrate as compared with said regions under the openings, is clearly illustrated in figure 1 of Sakamoto.

2. Appellant argues that it would not be obvious to form the metal wiring electrodes 17, 18 of Sakamoto over the entire substrate, because neither one of them could be formed over the entire substrate without subsuming the other and completely changing the structure of Sakamoto, and still function as different electrodes.

The conventional method of forming metal electrodes over a device is by depositing a metal layer over the entire device, and then etching openings in the metal layer in order not to short circuit the device and in order to provide separation between the various parts of the device. Thus, depositing the metal wiring layer over the entire substrate in Sakamoto's device and etching openings in order to obtain two separate wiring layers 17 and 18, would not result in one wiring layer subsuming the other and changing the structure of Sakamoto. The two wiring electrodes in Sakamoto's device would still function as two different electrodes.

Furthermore, it would be simpler to deposit the metal wiring layer over the entire substrate and etch the required openings, than complicating the processing steps of making the device by providing special masks in order to repeatedly form sections of metal wiring layers over selected sections of the substrate. Therefore, it would be obvious for an artisan to form the metal wiring layer over the entire substrate, as claimed.

Moreover, figure 1 of appellant depicts an aluminum wiring layer 29 sectioned by having openings therein, wherein each section 29 is used as source electrode. Sakamoto also uses an aluminum wiring layer 18, 19 sectioned by having openings therein. The only difference between appellant's aluminum wiring layer and Sakamoto's aluminum wiring layer is that Sakamoto uses sections 18, 19 as a base electrode and as an emitter electrode, respectively. However, the limitations recited in claim 9 do not prevent the metal wiring layer from performing different electrical functions.

3. Appellant argues that Sakamoto does not teach forming metal wiring electrodes over the entire substrate.

Claim 9 recites "a metal wiring layer located over the entire substrate except at openings above the regions irradiated, wherein radiating rays passing to the regions irradiated through the openings generate the crystal defects under the openings". This means, that the metal wiring layer can be located only over certain sections of the substrate, because the remainder of the substrate ("the entire substrate") can be considered the "openings". Therefore, when considering figure 1 of Sakamoto, the "openings" can be taken as the areas located left and right to metal wiring layer 17, 18 (until the edge of the substrate) together with the areas in between metal wiring layer 17, 18. Thus, Sakamoto teaches a metal wiring layer located over the entire substrate except at openings above the regions irradiated".

Regarding the claimed limitations of "radiating rays passing to the regions irradiated through the openings generate the crystal defects under the openings", the broad recitation of the claim does not require the radiating rays to generate the crystal defects under all the openings. Therefore, even if the openings which are located left and right to metal wiring layer 17, 18 (until the edge of the substrate, not depicted in figure 1 of Sakamoto), do not include crystal defects, Sakamoto still teaches radiating rays passing to the regions irradiated through the openings generate the crystal defects under the openings, because crystal defects are generated in openings in between metal wiring layer 17, 18.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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